REMARKS

The application contains claims 1-7, 9-23, and 26-36. Claims 6-7 are identified as reciting allowable subject matter. All other claims have been rewritten in independent form. In view of the following remarks, Applicants respectfully request allowance of the application.

At the outset, Applicants thank Examiners Padmanabhan and Inoa for the courtesy of the October 2, 2003 interview with the undersigned. At that interview, it was agreed that: 1) the previous office action should not have been marked final, 2) the cited prior art does not teach or suggest independently addressable cachelets and 3) the cited prior art does not teach or suggest cachelet pointers and conflict resolution among them. The following arguments largely repeat the arguments presented in the interview.

THE OFFICE ACTION SHOULD NOT HAVE BEEN FINAL.

At the interview, it was agreed that the prior office action (paper no. 10) should not have been made final. The office action included several new grounds of rejection that were not necessitated by any amendment. For example, claims 10 and 16 have not been amended during prosecution but were rejected over newly discovered prior art.

ALL CLAIMS DEFINE OVER THE ART

As discussed in the interview, the pending claims are allowable over the cited art because the prior art, even if considered in combination, do not teach or suggest independently addressable cachelets or conflict resolution among cachelet pointers.

The Prior Art Does not Teach or Suggest Independently Addressable Cachelets.

Claims 1-5 and 9-28 stand rejected as either anticipated by Maiyuran (U.S. 2000/0129201) or obvious over it and a secondary reference, Gruber (U.S. Patent No. 6,115,793). Applicants respectfully request withdrawal of these grounds of rejection because the cited art fails to teach or suggest all elements of the pending claims.

Consider claim 1. It recites:

> A cache, comprising a plurality of independently addressable cachelets, each cachelet to provide data responsive to independent load requests in a single clock cycle.

Maiyuran does not teach this subject matter. Even if it were proper to consider Maiyuran's ways as cachelets, Maiyuran's disclosure clearly establishes that the ways are not independently addressable. Maiyuran states:

> The address decoder 140 may have a plurality of outputs, one connected to each of the N cache entries 110 in each of the ways... The decoder output labeled "set0," for example, may be connected to one cache entry 110 from each of the ways in the cache 100. Similarly, all other output lines from the decoder 140 may be connected to one cache entry 110 from each ways... ***In response to an address signal $ADDR_{set}$, the decoder 140 may enable W cache entries 110, where W represents the number of ways in the cache 100.***

Maiyuran, ¶ 0015. Instead of having independently addressable cachelet, Maiyuran clearly discloses that each way in his cache is addressed using a ***common*** address signal $ADDR_{set}$. Maiyuran further does not disclose each cachelet providing data responsive to independent requests. Thus, Maiyuran does not anticipate claim 1. The rejections to claims 1-5, therefore, should be withdrawn.

Claim 19 also defines over the art. It recites:

> A cache comprising: a plurality of independently addressable cachelets, [and] means for distributing independent loads to each of the cachelets in a single clock cycle.

Maiyuran does not disclose this subject matter either. As noted above, Maiyuran's various ways are not independently addressable. They are addressed in unison, using a common ADDRset address. Further, Maiyuran does not disclose independent loads being distributed to each of his ways. There is a single request made to the cache, using the ADDR address (of which ADDRset is part). Maiyuran simply has no relevance to the claimed subject matter. Applicants therefore request withdrawal of the rejections to claims 19-21.

Claim 22 also stands rejected as anticipated by Maiyuran. It, too, defines elements that are neither taught nor suggested by the cited art, including:

> a first layer of cache, comprising a plurality of independently addressable cachelets and means for distributing multiple loads among the cachelets in a single clock cycle, and

a second layer of cache to receive a load that misses the cachelet to which it was assigned.

As noted, Maiyuran does not teach or suggest 1) independently addressable cachelets or 2) multiple loads distributed among the cachelets. Further, as explained in the interview, it is not appropriate to consider Maiyuran's ways to correspond to different layers of cache. Instead, they correspond to different cache levels (e.g., level 1, level 2 in some architectures). Claims 22-25, therefore, define over the cited art.

The Cited Art Does not Teach or Suggest Cachelet Pointers or Conflict Resolution.

As argued during the interview, the cited art does not teach or suggest use of cachelet pointers or conflict resolution among them. Accordingly, Applicants request withdrawal of the rejections to claims 10-18 and 26-28.

Claim 10 recites, for example:

determining whether any of the cachelet pointers conflict with any other cachelet pointers,
if a conflict occurs among cachelet pointers, forwarding one of the data requests associated with a conflicting cachelet pointer to the identified cachelet, and
reassigning data requests associated with remaining conflicting cachelet pointers to unused cachelets.

The cited art does not teach or suggest such subject matter. As noted, Maiyuran discloses a set associative cache with multiple ways but there is no routing of requests among them. A common address value ($ADDR_{set}$) is input to every way. Gruber discloses a system in which logical cache address are distributed among a variety of physical cache locations. No reference discloses any system in which a plurality of cachelet pointers are checked to determine if a conflict exists and, if so, to send one of the requests to the identified cachelet and reassign other requests to other cachelets. Claims 10-13, therefore, define over the art.

Claim 14 recites:

determining whether any of the cachelet pointers conflict with any other cachelet pointers,
forwarding non-conflicting data requests to a cachelet identified by the cachelet pointer,
for the conflicting data requests, forwarding one of the conflicting data requested to the identified cachelet and

reassigning remaining conflicting data requests to unused cachelets.

Again, the cited art does not teach or suggest this subject matter. Maiyuran does not disclose forwarding data requests individually to cachelets. Gruber does not disclose use of cachelet pointers, forwarding of non-conflicting data request or reassigning of conflicting data requests. Thus, claims 14-15 define over the art.

Claim 16 recites:

determining whether any of the cachelet pointers are valid,

forwarding data requests having valid cachelet pointers to the addressed cachelet, and

assigning remaining data requests to unused cachelets according to a default assignment scheme.

No reference determines whether a cachelet pointer is valid. Further, no reference forwards a data requests to a cachelet using a cachelet pointer or reassigns data requests to unused cachelets. Claims 16-18 also are allowable over the prior art.

NEW CLAIMS

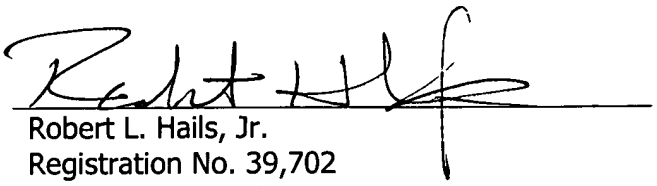
New claims 29-36 are presented. New independent claim 34 recites directing data requests to various cachelets in unison, which is neither taught nor suggested by any prior art reference. Claims 29-33 depend from independent claims discussed above and, therefore, are allowable over the prior art.

CONCLUSION

All rejections have been overcome. Applicants respectfully request allowance of the application.

Respectfully submitted,

Date: October 2, 2003



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